AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. **(currently amended)** A data [[Data]] access apparatus, comprising:

an external memory unit for storing data, wherein the external memory unit has a second time cycle for performing a task; and

a control unit coupled ~~couples~~ with the external memory unit via a memory bus, said control unit comprising:

a microprocessor unit, having a first time cycle to perform a microprocessor operating; and

a memory interface control unit for correspondingly transforming an internal data access address of an internal memory unit, which is accessible only by the microprocessor unit, into a data address of the external memory unit, thereby the microprocessor unit issuing the internal data access address could access data from the external memory unit via the memory interface control unit;

wherein

the external memory unit has a data segment storing flow control parameters and numerical arithmetic of the microprocessor ~~operating~~ unit, and

when the microprocessor unit attempts ~~is going~~ to access the data segment storing flow control parameters and numerical arithmetic from the external memory unit, an access request signal issued from the control unit associated with the microprocessor unit against another device [[for]] accessing the external memory unit is directed to the external memory unit, and the first time

cycle is suspended until an acknowledge signal indicating that ~~illustrative of~~ the microprocessor unit may access the data segment of the external memory unit is received.

2. (previously presented) The data access apparatus according to claim 1, wherein the first time cycle is longer than the second time cycle.

3. (previously presented) The data access apparatus according to claim 1, wherein the first time cycle is revived from suspending when the second time cycle is finished.

4. (previously presented) The data access apparatus according to claim 3, wherein the duration suspending the first time cycle is a time when the external memory unit finishes a current task.

5. (original) The data access apparatus according to claim 1, wherein the external memory unit is a dynamic random access memory (DRAM).

6. (original) The data access apparatus according to claim 1, wherein a capacity of the data segment of the external memory unit is smaller than a capacity of the external memory unit.

7. (original) The data access apparatus according to claim 1, wherein the data access apparatus could be applied to an optical-electronic system and which is selected from: a CD-ROM, CD-RW, DVD+/-ROM, DVD+/-RW.

8. **(currently amended)** A control unit for accessing data from ~~of data access with couples to~~ an external memory unit, having a second time cycle ~~for performing a task~~, via a memory bus [[for]] in an optical-electronic system, the control unit ~~of data access~~ comprising:

a microprocessor unit having a first time cycle to perform a microprocessor operation; and

a memory interface control unit for correspondingly transforming an internal data access address of an internal memory unit, which is accessible only by the microprocessor unit, into a data address of the external memory unit, thereby the microprocessor unit issuing the internal data access address could access data from the external memory unit via the memory interface control unit; [[and]]

~~a microprocessor unit having a first time cycle to perform a microprocessor operation,~~ wherein

when the microprocessor unit attempts ~~is going~~ to access data from the external memory unit via the memory interface, the control unit is operable to [[would]] send an access request signal to the external memory unit,

~~wherein~~ flow control parameters and numerical arithmetic of the microprocessor unit ~~operating~~ is stored in a data segment within the external memory unit, and

when the microprocessor unit attempts ~~is going~~ to access the data segment storing flow control parameters and numerical arithmetic from the external memory unit, the access request signal issued from the control unit associated with the microprocessor unit against another device [[for]] accessing the external memory unit is directed to the external memory unit, and the first time cycle is suspended until an acknowledge signal indicating that ~~illustrative of~~ the microprocessor unit may access the data segment of the external memory unit is received.

9. (previously presented) The control unit of data access according to claim 8, wherein the first time cycle is longer than the second time cycle.

10. (previously presented) The control unit of data access according to claim 8, wherein the first time cycle is revived from suspending when the second time cycle is finished.

11. (previously presented) The control unit of data access according to claim 10, wherein the duration between the first time cycle suspended and revived is a time when the external

memory unit finishes a current task.

12. (original) The control unit of data access according to claim 8, wherein the external memory unit is a DRAM.

13. (original) The control unit of data access according to claim 8, wherein a capacity of the data segment of the external memory unit is smaller than a capacity of the external memory unit.

14. (original) The control unit of data access according to claim 8, wherein the optical-electronic is selected from: a CD-ROM, a CD-RW, a DVD+/-ROM, and DVD+/-RW.

15. **(currently amended)** A data access method used in a control unit for accessing data in an external memory unit, said method comprising:

correspondingly transforming an internal data access address of an internal memory unit, which is accessible only by a microprocessor unit of the control unit, into a data address of the external memory unit, thereby the microprocessor issuing the internal data access address could access data from the external memory unit;

suspending a first time clock used by [[a]] the microprocessor of the control unit when the microprocessor sends an access request signal for accessing a data segment in the external memory unit, wherein the data segment stores flow control parameters and numerical arithmetic of the microprocessor ~~operating~~ unit, and wherein the access request signal issued from the control unit associated with the microprocessor unit against another device [[for]] accessing the external memory unit is directed to the external memory unit; and

reviving the first time clock when an acknowledge signal indicating that ~~illustrative of~~ the microprocessor unit may access the data segment of the external memory unit is received.

16. (previously presented) The data access method according to claim 15, wherein the external memory unit has a second time cycle which is a time for accessing data stored in the external memory unit.

17. (previously presented) The data access method according to claim 16, wherein the first time cycle is longer than the second time cycle.

18. (previously presented) The data access method according to claim 16, wherein duration of the first time cycle between being suspended and being revived is a time of the second time cycle being finished.

19. (previously presented) The data access method according to claim 15, further comprising the external memory unit performs a current task when suspending the first time cycle, and after finishing the current task, reviving the first time cycle immediately.

20. (original) The data access method according to claim 15, wherein the method could be applied to an optical-electronic system which is selected from: a CD-ROM, a CD-RW, a DVD+/-ROM, and a DVD+/-RW.